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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/434,394	11/04/1999	JOHN S., YATES JR.	114596-20-4009	3898

38492 7590 12/28/2005

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EXAMINER	
NGUYEN BA, HOANG VU A	
ART UNIT	**PAPER NUMBER**
2192	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/434,394	YATES ET AL.	
	Examiner	Art Unit	
	Hoang-Vu A. Nguyen-Ba	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59 and 61-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,40-59 and 61-65* is/are allowed.

6)☒ Claim(s) *2,9,10,12-14,19-22 and 30* is/are rejected.

7)☒ Claim(s) *3-8,11,15-18,23-29 and 31-39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/23/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment filed September 23, 2005.

2. Claims 1-59 and 61-65 remain pending.

Priority

3. The priority date considered for this application is August 30, 1999, filing date of the parent application no. 09/385,394.

Information Disclosure Statement

4. The Office acknowledges receipt of the Information Disclosure Statement filed September 23, 2005. It has been placed in the application file and the information referred to therein has been considered.

Response to Amendments

5. Per Applicants' request, amendment to Claim 7 has been entered.

Response to Arguments

6. Applicants' arguments with respect to Claims 1-59 and 61-65 have been considered but are moot in view of new ground(s) of rejection.

Claim Rejections - 35 USC §112

7. The following is a quotation of the first paragraph of 35 U.S.C. §112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claim 14 is rejected under 35 U.S.C. § 112, first paragraph, as being single means claim. MPEP 2164.08(a).

A single means claim, i.e., where a means recitation does not appear in combination with another recited element of means, is subject to an undue breath rejection under 35 U.S.C. § 112, first paragraph. *In re Hyatt*, 708 F 2.d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983) (A single means claim which covered every conceivable means for achieving the stated purpose was held nonenabling for the scope of the claim because the specification disclosed at most only those means known to the inventor.). When claims depend on a recited property, a fact situation comparable to *Hyatt* is possible, where the claims cover every conceivable structure (means) for achieving the stated property (result) while the specification discloses at most only those known to the inventor.

In the instant application, Claim 14 covers every conceivable structure (e.g., instruction execution circuitry) for achieving the stated purpose of evaluating, based at least in part on an annotation encoded in a segment descriptor, whether an individual memory-reference instruction (or an individual memory reference of an instruction), references a device with a valid memory address that cannot be guaranteed to be well-behaved while the specification discloses at most only those known to the inventor.

Furthermore, it should be noted that although Claim 14 is interpreted in light of the specification, the limitations of the instruction execution circuitry described in the specification will not be read into Claim 14. Accordingly, any arguments that the limitations described in the specification provide patentable distinction over the prior art will be unpersuasive.

9. The following is a quotation of the second paragraph of the 35 U.S.C. § 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 2 is rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: producing a stream of instructions, generating memory references, determining whether or not memory addresses are guaranteed to be well-behaved, annotating in the instructions the results of the determining step, encoding and storing the annotation in a segment descriptor. These omitted steps are considered critical and essential because without the pre-performance of these steps, the claimed single step of evaluating is not operative. Alternatively stated, it is unclear as to how the evaluating step could be performed without the existence of a stream of instructions, the execution of which generates memory references, the existence of annotation stored in a segment descriptor that indicates whether or not the address where a device is located in the memory system is an address that cannot be guaranteed to be well-behaved.

11. Claim 14 is rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are at least: a device, a storage medium, a binary translator software and a circuitry to raise an exception. The existence and thus the claim of a device that is associated with the instruction execution circuitry are considered essential and critical for the instruction execution circuitry to be able to reference. The existence and thus the claim of a storage medium are essential and critical to provide the device with a storage area having an address. The existence and thus the claim of a binary translator software are essential and critical in order to generate the memory-reference instruction,

provide a segment descriptor to encode an annotation and to give an indication whether or not the memory address of the device is valid and guaranteed to well-behaved. A claim to a circuitry without the above-mentioned elements software is considered incomplete, non-enabling and devoid of any utility.

Double Patenting

12. The non-statutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper time wise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ 2d 2010 (Fed. Cir. 1993); *In re Long*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1993); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Voge*, 422 F2.d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F2.d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.103(c) 1.321(c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.37(b).

13. Claims 2+3 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 4+7 of '379 Patent in view of U.S. Patent No. 5,926,484 to Takusagawa.

Instant Claims 2+3	Patent/Copending Claims 4+7
2. A method, comprising the step of:	

for memory references generated as part of executing a stream of instructions on a computer, evaluating whether an individual memory reference of an instruction references a device having a valid memory address but that cannot be guaranteed to be well-behaved, based at least in part on an annotation encoded in a segment descriptor.	
	issuing a successful memory reference from a computer CPU to a bus;
	recording in a storage of the computer whether a device accessed over the bus by the memory reference is well-behaved memory or not well-behaved memory
3. A method of claim 2, further comprising the step of:	7. The method of claim 4, further comprising the steps of:
if the reference cannot be guaranteed to be well-behaved, re-executing the instruction in an alternative execution mode.	evaluating whether an individual memory reference of an instruction references a device that cannot be guaranteed to be well-behaved, and if the reference cannot be guaranteed to be well-behaved, re-executing the

	instruction in an alternative execution mode.

A question of patentability is raised with respect to representative Claims 2+3 of the instant application under the judicially created doctrine of "obviousness-type" double patenting with respect to '379 Patent Claims 4+7 (note that Applicants' argument – page 2 – incorrectly refers to '379 Patent Claims 4+78) in view of U.S. Patent No. 5,926,484 to Takusagawa.

Takusagawa discloses a device having a valid memory address (see at least Claim 9, first address register storing a valid address), issuing a successful memory reference from a computer CPU to a bus (see at least Claim 8, first stage for receiving a request issued by a processor for accessing a memory) and recording in a storage of the computer whether a device accessed over the bus by the memory reference is well-behaved memory or not well-behaved memory (see at least Claim 12, resetting first valid register to an invalid state – i.e., *recording in a storage of the computer* – when no fault is detected, i.e., *well-behaved memory* and resetting a third valid register to an invalid state and setting a pending register to a pending state when a fault is detected, i.e., *not well-behaved memory*).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to add the above steps taught by Takusagawa to the '379 Patent teachings as this would provide the '379 Patent teachings with necessary information to determine whether a memory is well-behaved or not well-behaved for the purpose of making appropriate corrections to improve system reliability and performance as suggested by Takusagawa (1:39-42).

14. A question of patentability is raised with respect to Claim 22 of the instant application under the judicially created doctrine of "obviousness-type" double

patenting with respect to '379 Patent Claims 4+8 in view of U.S. Patent No. 5,926,484 to Takusagawa.

'379 Patent Claims 4+8 contain every element of instant Claim 22 (i.e., **anticipate** Claim 22) except the limitation *based at least in part on an annotation encoded in a segment descriptor, and aborting the identified memory load* and *based at least in part on the identifying* (it should be noted that although '379 Patent Claims 4+8 contain the additional steps (e.g., of issuing and of recording) as pointed out by Applicants, an important issue that needs to be considered is that Patent Claims 4+8 **anticipate** every limitation of Instant Claim 22, except the above-mentioned limitations).

However, Takusagawa discloses the limitations *based at least in part on an annotation* and *on the identifying*. See at least 2:40-43 and discussion hereinafter in conjunction with the rejection of Claims 2 and 14 under 35 U.S.C. § 102 (a) as being anticipated by Takusagawa. The limitation *aborting the identified memory load* is also disclosed by Takusagawa in the Abstract, lines 6-7, e.g., "the processing of the request is suppressed by a pending register," and related text in the specification.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to add the above steps taught by Takusagawa to the '379 Patent teachings as this would provide the '379 Patent teachings with necessary information to determine whether a memory is well-behaved or not well-behaved for the purpose of making appropriate corrections to improve system reliability and performance as suggested by Takusagawa (1:39-42).

15. A question of patentability is raised with respect to Claim 30 of the instant application under the judicially created doctrine of "obviousness-type" double patenting with respect to '379 Patent Claims 4+8 in view of U.S. Patent No. 5,926,484 to Takusagawa.

'379 Patent Claims 4+8 contain every element of instant Claim 30 (i.e., **anticipate** Claim 30) except the limitation *instruction execution circuitry* and *based at least in part on an annotation encoded in a segment descriptor* (it should be noted that although '379 Patent Claims 4+8 contain the additional steps (e.g., of issuing and of recording) as pointed out by Applicants, an important issue that needs to be considered is that Patent Claims 4+8 **anticipate** every limitation of Instant Claim 30, except the above-mentioned limitations).

However, Takusagawa discloses the limitations *based at least in part on an annotation.* See at least 2:40-43 and discussion hereinafter in conjunction with the rejection of Claims 2 and 14 under 35 U.S.C. § 102 (a) as being anticipated by Takusagawa. The limitation *instruction execution circuitry* is also disclosed by Takusagawa in FIG. 1 and related text.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to add the above features taught by Takusagawa to the '379 Patent teachings as this would provide the '379 Patent teachings with necessary information and circuitry to determine whether a memory is well-behaved or not well-behaved for the purpose of making appropriate corrections to improve system reliability and performance as suggested by Takusagawa (1:39-42).

Claim Rejections - 35 USC § 101

16. 35 U.S.C. § 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the condition and requirements of this title.

17. Claims 2, 10 and 13 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

Under the most recent Federal Circuit cases, transformation of data by a machine (e.g., a computer) is statutory subject matter provided the claims recite "practical application, i.e., 'a useful, concrete and tangible result.'" State St Bank & Trust Co. v. Signature Fin. Group, Inc., 149 F.3d 1368, 1373, 47 USPQ 2d 1596, 1600-01 (Fed. Cir. 1998).

In this instant application, the language of Claim 2 raises a question as to whether this claim is merely directed to an abstract idea that is not tied to a machine which would result in a practical application producing a concrete, useful, and tangible result to form the basis for a statutory subject matter under 35 U.S.C. § 101.

The Office's interpretation of Claim 2 is that this claim does not expressly or implicitly recite any **transformation** of data by a machine. Structure will not be read into the claims for the purposes of the statutory subject matter analysis although the steps might be capable of being performed by a machine.

The single step of evaluating whether an individual memory reference of an instruction references a device having a valid address... based at least in part on an annotation encoded in a segment descriptor does not expressly or implicitly indicate any **transformation** of any **data**. Furthermore, this step does not specifically or implicitly require performance of the step by a machine in order to produce useful, concrete and tangible results as formulated in State Street case law.

Claims 10 and 13, which depend from Claim 2, are also rejected under 35 U.S.C. § 101 for the same reasons.

18. Claim 14 is rejected under 35 U.S.C. § 101 because the claimed invention is inoperative and therefore lacks utility.

Claim 14 recites a computer comprising instruction execution circuitry **designed** to evaluate, based at least in part on an annotation encoded in a segment descriptor, whether an individual memory-reference instruction ... references a device with a valid memory address... The Office's interpretation of Claim 14 is that this claim only recites an instruction execution circuitry **designed** to evaluate a certain instruction. Claim 14 does not expressly or implicitly require the instruction execution circuitry to actually perform the act of evaluating since the language of the claim only indicates that the circuitry is **designed** to perform the evaluation. Without any act being performed, the claimed invention lacks utility.

19. Claim 14 is rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

A claim that recites a computer without a computer program encoded on a computer-readable medium to instruct the computer to perform a certain process does not define structural and functional interrelationships between the computer (which permits the computer program's functionality to be realized) and the computer program and is thus not statutory. *Warmerdam*, 33 F.2d at 1361, 31 USPQ 2d at 1760. *In re Sarkar*, 588 F.2d 1330, 1333, 200 USPQ 132, 137 (CCPA 178). See MPEP §2106 (IV)(B)(1)(a).

Claims 19-21, which depend from Claim 14, are also rejected under 35 U.S.C. § 101 for the same reasons.

Claim Rejections - 35 USC § 102

19. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejection under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or foreign country, before the invention thereof by the applicant for patent.

20. Claims 2, 9, 12 and 14 are rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 5,926,484 to Takusagawa.

Claim 2

Takusagawa discloses at least a method, comprising the step of (see at least FIG. 1 in conjunction with FIG. 5 and related text):

for memory references generated as part of executing a stream of instructions on a computer (see at least 4:36-38), *evaluating* (see at least 2:50-62) *whether an individual memory reference of an instruction* (4:36-38; wherein the *individual memory reference of an instruction* is interpreted to mean address of the request) *references a device having a valid memory address but that cannot be guaranteed to be well-behaved, based at least in part on an annotation encoded in a segment descriptor* (see at least 2:40-43; *valid memory address* is indicated by a 1 in the valid field, *cannot be guaranteed to be well-behaved* is indicated by 0 in the clean field).

Claim 9

The rejection of base claim 1 is incorporated. Takusagawa further discloses *wherein the device having a valid memory address has an address in an I/O space of the computer* (see at least FIG. 1, e.g., the store-in cache memory).

Claim 12

The rejection of base claim 1 is incorporated. Takusagawa further discloses *wherein the segment descriptor is stored in a segment register* (see at least FIG. 1, e.g., the valid register).

Claim 14

Since Claim 14 recites a computer that performs the same method step of Claim 2, the same rationale set forth in the rejection of Claim 2 also applies to the rejection of Claim 14.

Allowable Subject Matter

21. Claims 3-8, 10-11, 13, 15-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

22. Claims 1, 40-54, 55-59 and 61-65 are allowed.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Vu "Antony" Nguyen-Ba whose telephone number is (571) 272-3701. The examiner can normally be reached on the following days of a bi-week: Monday-Thursday (first week) and Tuesday-Friday (second week) from 7:15 am to 5:45 pm.

If attempts to reach the examiner are unsuccessful, the examiner's supervisor, Tuan Dam can be reached at (571) 272-3695.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

Hoanguan Antony Nguyen-Ba

ANTONY NGUYEN-BA
PRIMARY EXAMINER

December 21, 2005